Journal of Undergraduate Research at Minnesota State University, Mankato

Volume 11 Article 5

2011

Optimization of Reactive Ion Etching (RIE) Parameters for Selective Removal of MOSFET Gate Dielectric and Evaluation of its Physical and Electrical Properties

Hojoon Lee
Minnesota State University, Mankato

Samuel Wood
Minnesota State University, Mankato

Optimization of Reactive Ion Etching (RIE) Parameters for Selective Removal of MOSFET Gate Dielectric and Evaluation of its Physical and Electrical Properties

Hojoon Lee, *Student Member, IEEE*, Samuel C. Wood, Muhammad A. Khaliq, *Senior Member, IEEE*

***Abstract*—The integrated circuit (IC) is dominated by technology using Complementary Metal-oxide-Semiconductor Field-effect Transistor (CMOSFET). In order to put over 300 million transistors on silicon chip requires selective removal of material by Reactive Ion Etching (RIE) which ensures vertical cut thereby increasing packing density of devices on the chip. The gate insulator of CMOS devices plays a crucial role in its electrical performance. In this research gate insulator of MOSFET has been etched by state-of-art technique RIE and its physical and electrical properties have been measured. The gate insulator etching by RIE give rise to charge accumulation on the gate dielectric resulting in change in threshold voltage. Also early breakdown of MOS devices is a direct consequence of charge accumulation on gate dielectric during RIE process. The RIE etching was performed with Technics Series 85-RIE unit, and it was optimized in respect of power, pressure, and composition of gases to achieve less charge accumulation, and stable threshold voltage. The thickness of the gate insulator was measured by the Nanospec before and after etching. Charges accumulated on gate oxide were measured by HP 4280A which is a high frequency capacitance-voltage (CV) measurement system. Annealing of the RIE etched gate oxide were performed at suitable temperature to bring the charges to minimum level. Results of the research are presented in tables and figures.**

***Index Terms*—charge accumulation, CV characteristics, CV characteristic adjustment, gate dielectric, mercury probe, dry etching, annealing, Reactive Ion Etching, threshold voltage adjustment**

Manuscript received Sep 1, 2011. This research work was supported by the Department of Electrical and Computer Engineering and Technology, Minnesota State University Mankato. This research journal was written after Undergraduate Research Conference (URC) on April 4, 2011 for session 2 which was held at 9:00am.

H. Lee is a senior in Department of Electrical and Computer Engineering and Technology, Minnesota State University Mankato, Mankato, MN 56001 USA with IEEE student member (e-mail: hojoon.lee@mnsu.edu).

S. C. Wood is a junior in Department of Electrical and Computer Engineering and Technology, Minnesota State University Mankato, Mankato MN 56001 USA (e-mail: sam.wood@mnsu.edu).

M. A. Khaliq is a professor in Department of Electrical and Computer Engineering and Technology, Minnesota State University Mankato, MN 56001 USA with IEEE senior member (e-mail: muhammad.khaliq@mnsu.edu).

I. Introduction

Wet etching was a major technique to implement etching process in the integrated circuit manufacturing in earlier days, but it has been changed to dry etching because of the two major reasons. First, dry etching is less hazardous to human than wet etching. The gate oxides were grown as silicon dioxide (SiO_2), it could be etched off with hydrofluoric acid (HF) which generates dangerous fumes, in wet etching. Also, it etches non-selected area of the devices. Second, the dry etching is anisotropic or directional etching so this method does not etch any other areas that were not selected besides wet etching (see Figure 1) etched all the ways that HF fumes reached [1], [2]. Hence, the dry etching will bring better results in etching quality and preferred use due to constant etching rate.

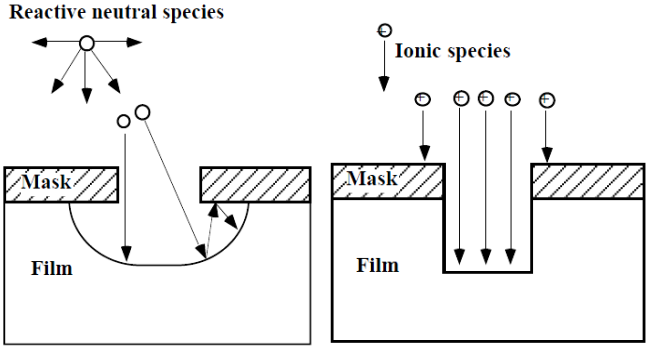

Fig. 1. Comparison of the etching region for wet and dry etching left and right respectively [1].

There are different dry-etching techniques. The mechanism of etching in each type can have a physical basis (e.g., in glow-discharge sputtering, or ion milling), a chemical basis (e.g., in plasma etching), or a combination of the two (e.g., what is termed RIE, or ion-enhanced etching) [3]. In this research, we use RIE system with tetrafluoromethane (CF_4) as an etchant. The schematic of RIE system is shown in Figure 2. The plasma generated accelerates the high energy ions of the gas by electromagnetic force and strikes the surface of the wafer stripping away the SiO_2. These molecules will react with accelerated ions and stick together. The used gas is pumped out of the system with an exhaust system.

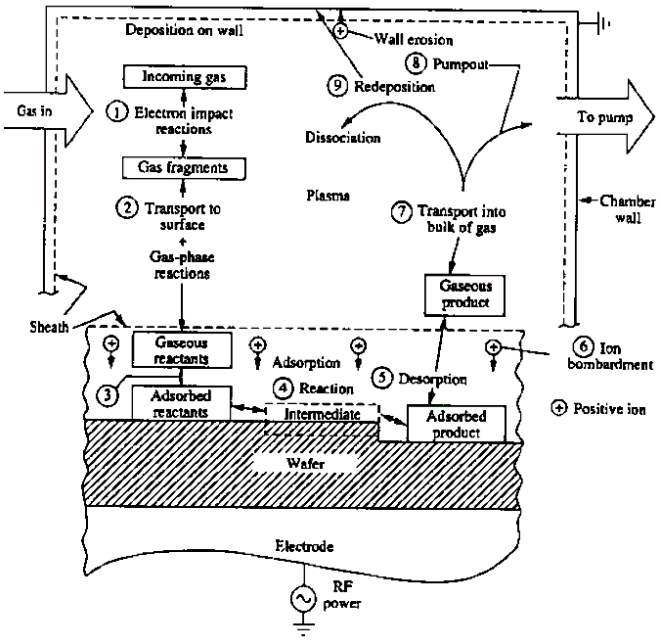

Fig. 2. Schematic view of the microscopic processes that occur during the etching of a silicon wafer [4].

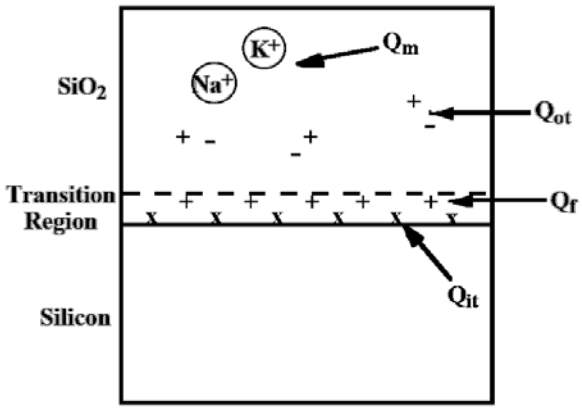

Fig. 3. Charges associated with the SiO_2/Si system, Q_{it} (charge defect at the Si/SiO_2 interface), Q_f (Fixed oxide charge), Q_{ot} (oxide trapped charge), and Q_m (mobile oxide charge) [1].

Since this method uses a high energy radio frequency (RF) signal, it weakens the chemical bonding at the interface of SiO_2 and Si and degrades the wafer characteristics. This charge defect at the Si/SiO_2 interface is called Q_{it}; it can interact with carriers during normal device operation by capturing or releasing holes and electrons, especially in very small MOS devices. This happens because of hot carrier effects, which can inject carriers into the gate dielectric. The Q_{it} states can be passivated through hydrogen annealing at fairly low temperatures (300-500°C). By passivation, the Q_{it} traps are bonded with H atoms, and they are no longer electrically active and no longer trap carriers [1].

Without the annealing process, Q_{it} goes untreated and increases the threshold voltage because of the trapped charges in the oxide layer. From Figure 4, the CV curve moves toward left side of the CV plot. In real device, the threshold should be positive voltage to perform as a MOSFET, so the gate dielectric needs to be controlled.

The concentrations of oxide trapped charge have been problems in the past, but modern processing methods for silicon have reduced them to levels small enough that they have a small effect on the device characteristics [5]. This problem can be fixed with annealing process which allows rebuilding the atomic structure, also can be observed on CV curve.

To adjust the CV curve and threshold voltage to the expected value, an annealing process was used. Annealing is a heat treatment process to repair the damaged chemical bonds between SiO_2 and Si interface. This process was short and wafers are heated up for 10 to 20 minutes; the threshold voltage will change based on the amount of time the wafers are in the oven.

The goal of the research was to optimize the RIE process and to evaluate the number of the charges added to the SiO2 layer. The effects of RIE and annealing process to the wafers were calculated by the parameters extracted from CV characteristics.

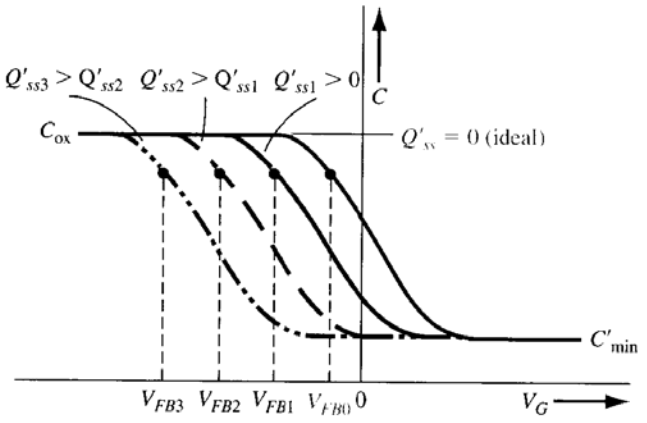

Fig. 4. CV curve variation with depending on the number of charges in the oxide layer [6].

II. Methodology & Data

A. Oxidation

Oxidation is the process of creating an insulator on the pure silicon wafer. Insulators are used to block contact of the substrate with other metals, materials or capacitive devices.

Twenty pure p-type silicon wafers were divided into five groups: group-A {A1-A4}, group-B {B1-B4}, group-C {C1-C4}, and group-E {E1-E4}. The oxide layers were grown by wet oxidation in 1000°C oven using water and oxygen (O_2). Each wafer group was given a specific amount of time to stay in the oven. Group-A was in the oxidation process for 15 minutes. The oxidation time for each group is located in Table 1.

The thickness of oxide layer was measured with a nanospectrometer and plotted in Table 1. The thicknesses were very close within the group, varying only by a few angstroms. The thickness increased roughly 500Å per 15 minutes. This oxidation process was marked as Phase1.

Group	Name	Mean (Å)	SD (Å)
A (15min)	A1	1074.10	14.25
	A2	1038.70	15.69
	A3	1064.60	13.32
	A4	1067.80	8.12
B (30min)	B1	1539.60	40.91
	B2	1606.70	43.23
	B3	1590.10	47.76
	B4	1630.58	53.16
C (45min)	C1	1989.50	45.54
	C2	2088.64	18.61
	C3	2031.70	34.01
	C4	2046.30	51.64
D (1hr)	D1	2561.32	50.28
	D2	2621.42	57.36
	D3	2669.32	43.70
	D4	2622.08	79.18
E (1hr 15min)	E1	2940.58	52.49
	E2	2936.72	36.20
	E3	2960.14	62.36
	E4	2957.56	50.27

Table. 1. Thickness of oxide for each group wafer after oxidation process.

B. Etching & RIE system optimization

To etch off the oxide in great quality, two parameters, pressure and power, are very important in dry etching techniques. The combinations of these values etch the oxide linearly which is called an etchant rate. The etchant rate determines the thickness of the oxide.

Fig. 5. RIE system in Microelectronics Fabrication Laboratory, Minnesota State University Mankato.

With the RIE system[1] in our lab (See Figure 5), the etchant rate and uniform etching was determined by several measurements with different settings. To run RIE system properly, preparation needs to be done by opening the gases which are nitrogen (N_2), O_2, and CF_4. Also, deionized water (DI water) and a vacuum pump must be turned on. N_2 is used for venting by controlling the vacuum chamber. CF_4 is used an etchant and to introduce high energy plasma inside of the RIE chamber. It is known that the addition of several percent O_2 to a CF_4 plasma dramatically increases the etch rate of Si and SiO_2 which is called "loading effect" [7], [8]. DI water allows the RIE machine to maintain a constant temperature during the etching process. After the preparation, the operation mode should be set to either auto or manual. Auto mode is a switch to turn on the machine after the parameters, power, pressure and time, are set to the correct values. Manual mode has the user manually track the time of the etching process. The Nanospec[2] measurements were done before and after etching to compare the thickness of oxide to determine the best condition for the etching process.

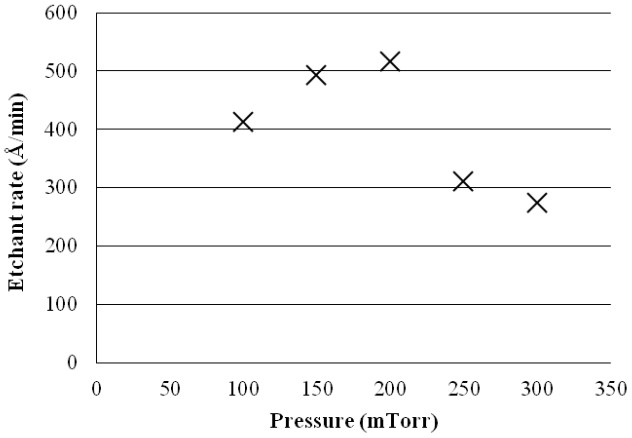

Fig. 6. Etchant rate with varying pressure in 200W.

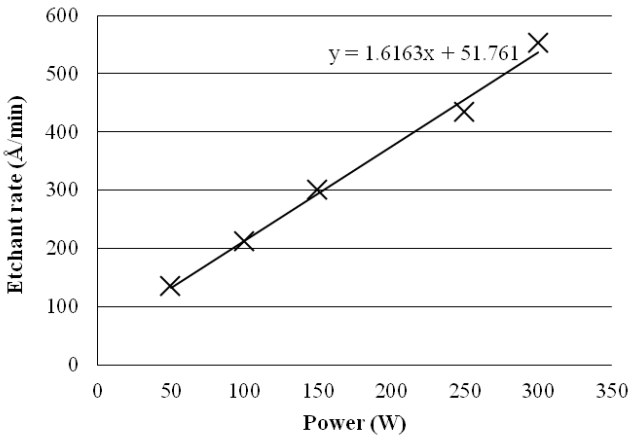

Fig. 7. Etchant rate with varying power in 250mTorr.

Figure 6 and Figure 7 were plotted with date gathered after several experiments to find the best condition for etching. First experiment, the power was at a fixed at 200W and the pressure was varied, shown in Figure 6. Second experiment is illustrated in Figure 7; the pressure was fixed at 250mTorr and the power was varied by 50W from 50W to 300W to find etchant rate. As a result, the pressure at 250mTorr and power at 100W produced the best uniformity etch across the wafer.

After optimizing the parameters for RIE, two wafers from each group were etched to about 200Å, which is typical thickness of the gate oxide of MOSFET integrated circuit

[1]Technics Series 85-RIE manufactured by Technics Inc. systems. (no longer business, filed chapter 7 in year 2002)

[2]Nanospec/AFT 3000 Series manufactured by Nanometrics.1550 Buckeye Drive, Milpitas, CA 95035

fabrication. From Table 2, most of the wafers were etched to a thickness of 200Å. The thickness of the oxide was measured with the Nanospec, non-oxide layer wafers were used as reference. The etching process was labeled as Phase2.

Group	Name	Mean (Å)	SD (Å)
A	A2	170.00	37.01
	A3	171.16	27.77
	A4	0.00	0.00
B	B1	0.00	0.00
	B2	88.22	23.30
	B3	82.10	31.84
C	C2	254.36	73.37
	C3	0.00	0.00
	C4	0.00	0.00
D	D2	255.92	43.88
	D3	0.00	0.00
	D4	165.74	37.93
E	E1	205.22	63.15
	E2	181.58	54.58
	E4	0.00	0.00

Table. 2. Thickness of oxide for each group wafer after etching process.

C. Annealing & Optimization

Annealing process is critical method to move the added charge down in the substrate and create a more stable device. The annealing process is a thermal heat treatment at a temperature of 600°C. To find the efficient time for the annealing process, group-A wafers were annealed 5, 10, and 15 minutes. At the time of 10 minutes, the number of charges per unit volume, calculated from the CV curve, was less than the number of charges per unit volume from the 5 and 15 minute times. The annealing process was marked as Phase3-1 for 5 minutes, Phase3-2 for 10 minute, and Phase3-3 for 15 minute process.

D. CV Measurement

To show the characteristics of each wafer, CV measurement was strictly used. CV characteristics curve were plotted with HP 4280A[3]. The data was imported from the Mercury probe[4] which has contact area of 0.1904cm^2. The contact area was calculated by the dimensions from the data sheet. All the wafers placed upside down to make contact, but also, the backside of wafers were etched with HF fumes to make contact on the substrate.

The voltage range was varying depending on the thickness of the oxide layer on the wafers; thicker oxide layer needed a wider voltage range to obtain the data of importance. The experimental typical voltage range was -20V to 10V.

E. Calculation

There were two important equations involved in the quantitative analysis. Eq. (1) is able to calculate maximum capacitance, C_{ox}, in the oxide layer with permittivity of free space, ε_o which is 8.854e-12F/m, and permittivity of SiO2, ε_r which is 3.9.

According to Eq. (2), total number charges, N_{ss}, in the oxide layer is equal to C_{ox} multiplied by the flatband voltage, ΔV, and divided by the charge of an electron, q. The flatband voltage is the point on the CV curve where the capacitance is $0.707C_{ox}$, and the charge of an electron is 1.602e-19C.

$$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} \quad (1)$$

$$N_{ss} = \frac{C_{ox}\Delta V}{q} \quad (2)$$

III. Results

Figure 8 shows the CV curve for every process for wafer A2. C_{ox} difference between Phase1 and Phase2 occurred by the etching process. According to Eq. (1), decreasing the thickness of the oxide increases C_{ox}. Phase3 was labeled as annealing process, Phase3-2 (10 minutes process) moved to the peak result. Phase3-3 (15 minutes process) went to back towards the left side of the graph. Hence, the 10 minute was a reasonable annealing time.

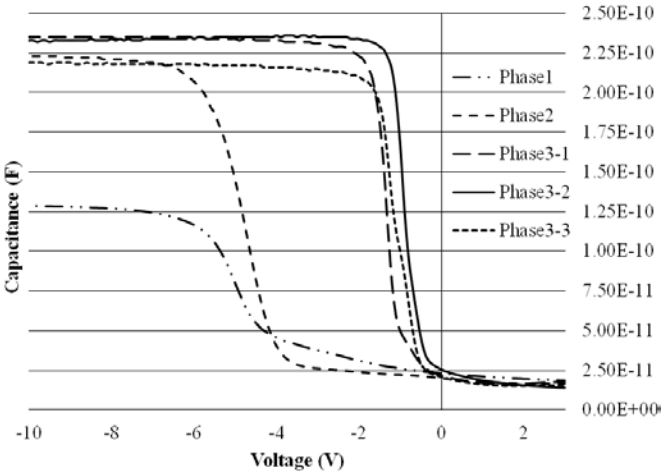

Fig. 8. CV characteristics adjustment of A2 for total process.

In Figure 9, 10, and 11 show only seven wafers because of damages or contaminations to the other wafers. Each graph represents the total number of charges per unit volume in the oxide layer depending on its thickness before, after etching process, and after annealing process respectively. From the graphs, the thinner oxides have more charges per unit volume because the same RIE and annealing process was applied to all different thicknesses of oxide. The trendline is showing the degree of changes.

The total number of charges per unit volume was dramatically increased about a hundred times after etching process, which means the etching process introduces a defect, Q_{it} and Q_o, in the interface of Si/SiO_2 and oxide layer. The data of Figure 11 indications the annealing process rebuilt the Si/SiO_2 bonding structure by decreasing the number of charges per unit volume by one order of magnitude.

[3]HP 4280A 1MHz C METER/C-V PLOTTER manufactured by Yokogawa-Hewlett-Packard Ltd. Takakura-Cho, Hachioji-Shi, Tokyo, Japan.

[4]Mercury Probe Model Hg-102 manufactured by MSI electronics. Woodside, New York 11377

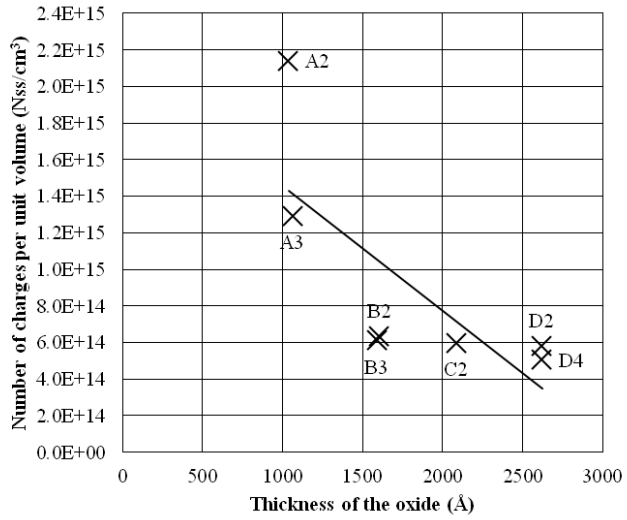

Fig. 9. Number of charges per unit volume versus thickness of the oxide before etching process.

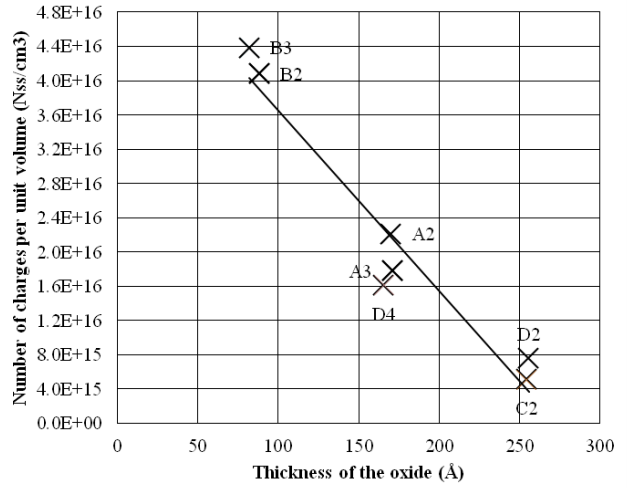

Fig. 10. Number of charges per unit volume versus thickness of the oxide after etching process.

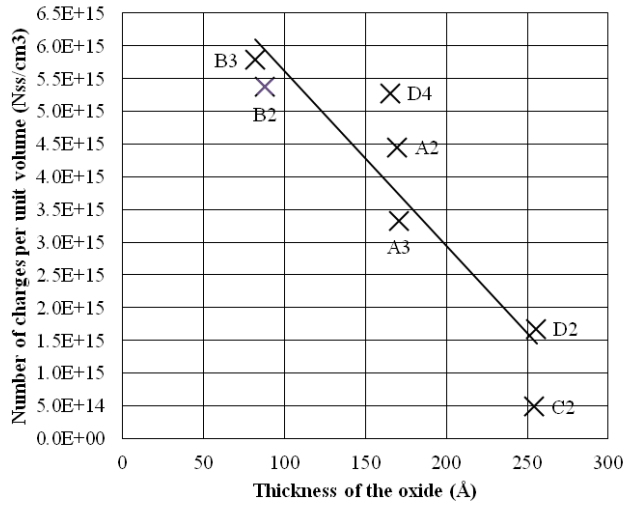

Fig. 11. Number of charges per unit volume versus thickness of the oxide after annealing process.

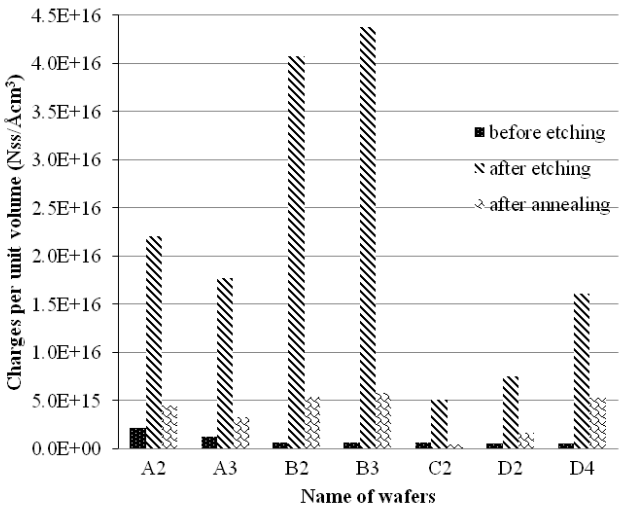

Fig. 12. Comparison of number of charges per unit volume for each process.

Figure 12 is a simplified graph to show the whole process with the number of charges in the oxide. After etching process, the number of charges was increased dramatically because of the high energy plasma. However, the number of charges was decreased after the annealing process. Therefore, the annealing process made the chemical bonding at interface of Si and SiO_2 stable.

IV. Conclusion

As concluding this research work, the CV characteristics curves in the experimental data mentioned above moved as predicted by the theory mentioned in Figure 2. RIE uses less time and gives better selectivity but, there was tradeoff with charge trapping inside of the oxide layer. To fix this problem, an annealing process was implemented. Further research work will include optimizing RIE machine correctly and annealing process. The etchant rate varied slightly with time and manually loading the wafers caused a different annealing time for each wafer set. There is possibility of error in calculating the charges per unit volume because the area of mercury contact might not be accurate as we calculated, since the number of electrons can be differ within very tiny area resulting in large error in total number of the trapped charges.

Acknowledgment

The authors wish to thank Dr. M. Khaliq who is our advisor and the faculty mentor during the research, and also Department of Electrical and Computer Engineering and Technology in Minnesota State University Mankato for providing Analytical, Wet Processing, and Microelectronics Fabrication laboratory.

References

[1] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology: fundamentals, practice and modeling.* Upper Saddle River, New Jersey: Prentice Hall, 2000, pp. 609, 624, 294, 352-357.

[2] B. A. Heath, "Selective Reactive Ion Beam Etching of SiO_2 over Polycrystalline Si", *J. Electorochem. Soc.*, vol. 129 (2), 1982, pp. 396-402
[3] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era: volume 1 – process technology.* Sunset Beach, CA: Lattice Press, 2000, pp. 666.
[4] G. S. Oehrlein and J. F. Rembetski, "Plasma-Based Dry Etching Techniques in Silicon Integrated Circuit Technology," *IBM J. Res. Devel.*, vol. 36 (2), 1992, pp. 140-157
[5] B. L. Anderson and R. L. Anderson, *Fundamentals of Semiconductor Devices.* New York, New York: McGraw-Hill, 2005, pp. 497.
[6] D. A. Neamen, *An Introduction to Semiconductor Devices*, New York, New York: McGraw Hill, 2006, pp.265
[7] C. J. Mogab, A. C. Adams, and D. L. Flamm, "Plasma etching of Si and SiO_2 – The Effect of Oxygen Additions to CF_4 Plasma," *J. Appl. Phys.*, vol. 49 (7), 1978, pp. 3796-3803
[8] T. Enomoto, M. Denda, and A. Yasuoka, "Loading Effect and Temperature Dependence of Etch Rate in CF_4 Plasma" *Jpn. J. Appl. Phys.*, vol. 18, 1979, pp. 155-163

Hojoon Lee (M'08) was born in Seoul, South Korea, in 1988. In 2007 he graduated in Internet Information Communication from Sunrin Internet High School, Seoul, South Korea and continued his education for a Bachelor of Science in Electrical Engineering from Minnesota State University Mankato.

He worked in Integrated Circuit Fabrication laboratory as a student helper in Spring 2010, and was Teaching Assistant for EE480/580 Integrated Circuit Fabrication laboratory in Fall 2011, Mankato, MN. His interested areas are Solid State Physics, Quantum Physics & Optics, Optoelectronics, and Nanofabrication.

Samuel C. Wood was born in Brooklyn Park, Minnesota in 1990. In 2008 he graduated from Champlin Park High School, Minnesota and is now attending Minnesota State University Mankato to pursuing a Bachelor of Science in Electrical Engineering.

Sam has been part of a research group that conducts research in the areas of analog design and device fabrication. The research group's latest project is using reactive ion etching to create metal oxide field effect transistor. His areas interests are analog design, micro and nanofabrication, and biomedical engineering.

Muhammad A. Khaliq (M'85–SM'91) He is Professor of Electrical and Computer Engineering in Department of Electrical and Computer Engineering and Technology at Minnesota State University, Mankato Minnesota. He is Director of the Microelectronics Fabrication Laboratory, and is with Minnesota State University, Mankato since 1988.